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DEC 16 2005

Response Under 37 C.F.R.§1.116
Expedited Procedure
Examining Group 1765

REMARKS

In the October 17, 2005 Office Action, the Examiner rejected all pending claims 1-2 and 4-20[1] of the present invention on various prior art grounds. Specifically, the Examiner rejected:

claims 1-2, 4-7, 9 and 11-16 under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,656,524 to Eklund et al. (hereinafter "Eklund");

claim 8 under 35 U.S.C. § 103 as allegedly unpatentable over Eklund in view of U.S. Patent No. 6,027,964 to Gardner et al. (hereinafter "Gardner");

claim 10 under 35 U.S.C. § 103 as allegedly unpatentable over Eklund in view of U.S. Patent No. 6,436,747 to Segawa et al. (hereinafter "Segawa"); and

claims 17-20 under 35 U.S.C. § 103 as allegedly unpatentable over Eklund in view of Segawa.

Applicants have hereby amended claims 1 and 17, from which claims 2, 4-16 and 18-20 depend, to define a specific processing sequence for carrying out certain processing steps recited therein.

Specifically, claim 1, from which claims 2 and 4-16 depend, has been amended to recite a step of "selectively performing an ion implant and an activation anneal in the at least one other type of device region forming at least one of an emitter of a bipolar transistor, a polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor," followed by a subsequent step of "forming a protective dielectric layer overlying said polysilicon layer in said at least one polysilicon resistor device region," which is in turn followed by a subsequent step of "providing a predetermined resistance value to said polysilicon layer in said at least one polysilicon resistor device region." Claim 17, from which claims 18-20 depend, has been amended to recite a step of "performing a rapid thermal anneal for an emitter/FET activation process on a wafer or chip having a partially formed polysilicon resistor having a polysilicon layer, said rapid thermal anneal forming at least one of an emitter of a bipolar transistor, a

[1] In the Office Action Summary page of the October 17, 2005 Office Action, it was stated that "Claim(s) 1-20 is/are pending in the application." However, claim 3 has been cancelled in the Response filed on August 4, 2005 (see page 2 of the August 4, 2005 Office Action). Therefore, only claims 1-2 and 4-20 are currently pending in the present application.

polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor," followed by a subsequent step of "depositing a protective layer over the polysilicon layer to protect the polysilicon layer against subsequent silicide processing," which is in turn followed by a subsequent step of "ion implanting a dopant into the polysilicon layer through the protective layer," which is further followed by a subsequent step of "performing silicide processing to form the precision polysilicon resistor."

Support for the above amendments to claims 1 and 17 can be found in paragraph [0019] of the present application. Since the above amendments to claims 1 and 17 do not introduce any new matter into the application, entry thereof is respectfully requested.

Applicants respectfully traverse the Examiner's prior art rejections of the amended claims 1-2 and 4-20, because none of the cited references teaches or suggests a method comprising processing steps that are carried out in the processing sequence as expressly recited by the amended claims 1-2 and 4-20.

Specifically, the primary reference by Eklund discloses a method of fabricating polysilicon resistors that have minimized parasitic capacitance, which are integrated with a bipolar transistor fabrication process. From the description provided in Eklund, a bipolar transistor is partially formed prior to fabricating the resistor. See Col. 3, line 57-Col. 4, line 23. After partially forming the bipolar transistor, the polysilicon for the resistor as well as the emitter is deposited. After deposition of the polysilicon in the resistor region, the polysilicon layer is implanted and then blocked with a patterned mask, followed by emitter implant. See Col. 4, lines 38-44. The patterned mask is present during implanting of the emitter. Annealing of the polysilicon emitter in the bipolar region and the polysilicon of the resistor then both takes place. See Col. 4, lines 44-48.

In contrast, the amended claims 1 and 17 of the present application, from which claims 2, 4-16, and 18-20 depend, recites formation of a component of an active device, such as an emitter of a bipolar transistor or a gate/source/drain of a field effect transistor (FET), by ion implantation

and/or annealing, prior to provision of the predetermined resistance value to the polysilicon layer (as recited by claim 1) or prior to implantation of a dopant into the polysilicon layer (as recited by claim 17) in the resistor device region.

Clearly, the Eklund reference discloses a method having a processing sequence that is significantly different from that recited by the amended claims 1-2 and 4-20 of the present application. Eklund thus fails to provide any derivative basis for Applicants' claimed method as recited by the amended claims 1-2 and 4-20.

The applied disclosure of the secondary references, Gardner and Segawa, cannot remedy the above-described deficiency of the primary reference Eklund.

Correspondingly, the claimed invention of the present application, which is directed to a method with processing steps carried out in a specific sequence as positively recited by the amended claims 1-2 and 4-20, patentably distinguishes over all the cited references.

Applicants respectfully request the Examiner to reconsider, and upon reconsideration to withdraw, the prior art rejections of claims 1-2 and 4-20.

CONCLUSION

Based on the foregoing, claims 1-2 and 4-20 as amended herein are in condition for allowance. Issue of a Notice of Allowance for the application is therefore requested. If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned attorney at (516) 742-4343 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,

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